Table 4-3 Write Access Limited Registers

Operating Modes	Register Address	Register Name	Must be Written in First 64 Cycles	Write Anytime
SMOD = 0	$x024	Timer Interrupt Mask 2 (TMSK2)	Bits [1:0], once only	Bits [7:2]
	$x035	Block Protect Register (BPROT)	Clear bits, once only	Set bits only
	$x039	System Configuration Options (OPTION)	Bits [5:4], Bits [2:0], once only	Bits [7:6], Bit 3
	$x03C	Highest Priority I-Bit Interrupt and Miscellaneous (HPRIO)	See HPRIO description	See HPRIO description
	$x03D	RAM and I/O Map Register (INIT)	Yes, once only	—
SMOD = 1	$x024	Timer Interrupt Mask 2 (TMSK2)	—	All, set or clear
	$x035	Block Protect Register (BPROT)	—	All, set or clear
	$x039	System Configuration Options (OPTION)	—	All, set or clear
	$x03C	Highest Priority I-Bit Interrupt and Miscellaneous (HPRIO)	See HPRIO description	See HPRIO description
	$x03D	RAM and I/O Map Register (INIT)	—	All, set or clear

4.2.2.1 CONFIG Register

The CONFIG register consists of an EEPROM byte and static latches that control the startup configuration of the MCU. The contents of the EEPROM byte are transferred into static working latches during reset sequences. The operation of the MCU is controlled directly by these latches and not by CONFIG itself. In normal modes, changes to CONFIG do not affect operation of the MCU until after the next reset sequence. When programming, the CONFIG register itself is accessed. When the CONFIG register is read, the static latches are accessed.

Operation of the CONFIG register in the MC68HC811E2 differs from other devices in the M68HC11 E series. Refer to the two descriptions of the CONFIG register.

CONFIG — System Configuration **$103F**

	Bit 7	6	5	4	3	2	1	Bit 0
	—	—	—	—	NOSEC	NOCOP	ROMON	EEON
RESETS:								
S. Chip:	0	0	0	0	U	U	1	U
Boot:	0	0	0	0	U	U(L)	U	U
Exp.:	0	0	0	0	1	U	U	U
Test:	0	0	0	0	1	U(L)	U	U