High-Performance, Low-Power and Low-Cost SoC Design Techniques for Consumer Electronics Products

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CHALLENGES IN THE EXPANDING DIGITAL WORLD

The Consumer Electronics Association (CEA) predicts that overall planned spending on consumer electronics (CE) products will be up 27 percent this holiday season. With the market's continued growth and the increasing focus on consumer electronics as "the next big thing", CE manufacturers and everyone in the food chain is feeling the pressure. The feature and time-to-market treadmills are getting steeper, and the technologies are becoming increasingly complex, while at the same time new CE products require greater performance and ease of use, as well as reduced power and cost. Couple this with the increasing reliance on silicon providers to address these issues, and it's clear why SoC designers are meeting significant challenges as the industry moves into the expanding digital world.

Although there are many variables when considering the design of a CE SoC, the typical engineer is faced with achieving four major objectives: delivering high-performance solutions with low power consumption, at a low cost and with shorter development time.

Issues that Affect Cost and Development Time

Time is money, so every moment spent on design and development equates to more costs. And, the greater number of features, the greater the time and expenses. Some of the issues affecting total time and cost include the choice of a semiconductor vendor, selection of a CPU-based or a multiprocessor-based solution, unproven solutions or unverified IP, and the lack of emulators or prototyping systems that allow customers to write software in parallel with hardware development.

An appropriate process technology must also be chosen. Project costs are skyrocketing as fabrication technology migrates to deeper-submicron processes. Developers may wish to choose a 90nm or a 65nm process to contain many complex functions in a single chip. However, this is a costly choice compared to a 0.13-micron process. So, careful evaluation must be made on the process technology.

Multiple CPU cores and IP licensing can increase time and costs associated with negotiating multiple licenses. The integration of multiple IP blocks from different vendors can be a complex process that may fatally lengthen the design and verification stages of an SoC project.

Issues that Affect Power Consumption

In portable-device designs, battery life is of prime concern, and low-power operation is mandatory. Some of the issues that affect dynamic power consumption include clock speed, feature complexity, pipeline depth, and efficiency of memory access. However as semiconductor process nodes advance to 90n and beyond, the leakage current from transistors becomes even more of a concern as they now have more weight on the total system power consumption. Some of the factors that affect the static power consumption are type of transistors being used, operating voltage, and total number of gates on the chip.

SELECTING THE RIGHT SOLUTION

One of the early decisions that can contribute greatly to addressing these key challenges is partnering with the right vendor to deliver the right solution that will provide the optimal balance of performance, power and cost. After reviewing a solution designed to just this, we'll look at the ways it has been optimized to address these challenges.

Let's examine the ZEVIO™ SoC-design platform from LSI Logic. The ZEVIO architecture enables turnkey, semi-customizable, and fully customizable ZEVIO solutions to address the cost, power, time-to-market, and feature-differentiation requirements of consumer electronics products, such as electronic toys, entertainment devices and GPS navigational systems

The ZEVIO platform includes hardware and software IP, emulators and prototyping systems, and design services. Using the emulators and prototyping systems, customers can write software while they are developing their hardware designs. Designs that are developed with the ZEVIO platform can be fabricated by LSI-affiliated foundries or any other foundries.

With a large library of pre-verified intellectual property (IP) blocks that are critical to developing consumer electronics products, the ZEVIO architecture enables products using proprietary or standardized IP to move from concept to prototype in as little as six months. Two or more CPU cores can be used in a single SoC. The architecture supports several 32-bit ARM and MIPS Technologies CPU cores and 16-bit ZSP® DSP cores. Up to 16 AMBA high-speed bus (AHB) masters can be included. Masters can either be CPUs, graphics processor units (GPUs), distributed bus units (DPUs), or anything that is able to drive the AHB bus by itself. A custom solution based on the ZEVIO architecture can significantly reduce manufacturing costs by consolidating multiple processors and functions onto a single chip.

How does the ZEVIO architecture deliver a high-performance solution that will enable reduce cost, power and time-to-market enough to enable sub-$150 CE products?

ADDRESSING COST AND DEVELOPMENT TIME

Because of the seasonality in the consumer business, missing a launch target window can lead to a disastrous consequence of delaying a business opportunity up to one full year. As the complexity of the system increase, the time it takes to architect, design and verify a chip is exponentially growing. In addition, the chances of getting the first silicon to production naturally increases since there are more potential for bugs as gate count increases. Therefore it is critical to have a sound methodology and easy to use design platform in order to minimize those risks and at the same time reduce the turn around time of developing the chip.

Pre-Verified IP

The ZEVIO architecture addresses this concern by defining the platform to be simple to use. In many cases, a pre-verified IP might work in a stand-alone environment but may run into issues when combined with multiple IPs due to lack of understanding by the designers in how to use them at the a total system architecture level. Incorrect configuration options such as bus type, miscalculating the memory bandwidth requirements, and even simple misconnections of signals are common errors designers not familiar with the IPs can run into. By basing the architecture of the system on ZEVIO, designers can simply plug the necessary IPs and can worry much less about IP integration issues. As a result, a ZEVIO-based turnkey design enables system designers to receive first silicon prototypes in as little as six months from the time when the specification is finalized.

Currently, the platform includes several general-purpose 32-bit processor cores, including the ARM7, ARM9, and ARM11 families and the MIPS32 24K, 5Kf, and 4K processors.

For signal processing, the ZEVIO architecture offers cores from the ZSP200, ZSP400, and ZSP500 families. All of the ZSP cores are 16-bit fixed-point DSPs with superscalar pipelining, so their signal-processing capabilities surpass the basic DSP extensions available with the ARM and MIPS processors.

Memory-controller cores can interface to SDRAM and NAND flash memory. Mobile DDR-DRAM is coming in the future. Peripheral IP includes I/O controllers popular in consumer-electronics products: USB 2.0 (including USB On the Go), IEEE 1394 Firewire, and Secure Digital I/O.

Mixed-signal components include a USB 2.0 physical-layer interface (PHY), power-management unit (PMU) regulators, and digital-to-analog converters (DAC) for video and stereo audio.

For graphics and sound, the ZEVIO architecture provides a new 2D/3D graphics engine and a new 64-channel sound-synthesis engine. The architecture includes an LCD controller for TFT and CSTN displays as well as video and audio software codecs for standards such as MPEG-4, H.264, and Voice over Internet Protocol (VoIP). By integrating a NTSC/PAL encoder and video DAC, a direct TV-out connection can be supported.

Support Tools and Software Development Savings

The ZEVIO platform includes prototyping systems that use extensive FPGAs and daughter cards. This enables software developers to start writing code prior to having silicon, allowing software and hardware developers to work in parallel, thus reducing total elapsed time for development and reducing project cost.

The FPGA prototyping system can be populated with up to three FPGAs. The system can be clocked at 24 to 48MHz, and it can simulate as many as two million ASIC-equivalent gates. Each FPGA socket has a daughtercard slot which can support a daughtercard with discrete components or mixed-signal blocks that cannot be emulated in FPGAs. The prototyping system and accompanying low-level software is available from third parties.

The platform includes a real-time operating system, an embedded Linux operating system, 3D-graphics software, a web browser, and two debuggers and in-circuit emulators. Other operating systems can also be ported to the platform.

In developing the ZEVIO 3D graphics processor, LSI partnered with mobile entertainment hardware and software design experts from KOTO CO., Ltd.. Features were chosen based on interviews with game developers who were familiar with 3D graphics. Many of these functions were prioritized in order to reduce the software development cost.

Memory Controller

The ZEVIO platform supports a very efficient 20,000-gate, 12-port memory controller for 16-bit SDRAM. The controller interfaces to version 2.0 of the ARM Advanced Microcontroller Bus Architecture (AMBA). Comparable memory controllers from competing vendors typically require up to five times this number of gates. The ZEVIO memory controller accomplishes this efficiency by having no caches or FIFO buffers. Instead, it runs at two times the clock

speed of the AMBA High-speed Bus (AHB), and memory data is accessed in short bursts which read the minimum amount of data required by the AHB bus master. This approach avoids caching excess data that will not be needed. By pipelining control commands to memory, the device takes advantage of open command cycles without impeding traffic on the bus. The memory controller fetches two 16-bit words from memory on every AHB clock cycle. The controller can write data to nonconsecutive memory addresses without rearbitrating the AHB. By holding control of the AHB during the bursts, the controller can reduce the bus-arbitration latency by 70%.

ADDRESSING HIGH-PERFORMANCE AND LOW POWER

Power Management Unit

The ZEVIO power management unit (PMU) enables and disables clocks to each modules, shuts down and powers up PLLs, and allows software developers to fine tune optimal frequencies required to achieve optimal power-performance balance. Since the PMU runs on a special power island, the rest of the chip can be completely shut down to save leakage power while monitoring for wake-up events to turn the rest of the chip back on.

3D Graphics Processor

The ZEVIO platform has a new graphics engine that performs geometry operations. It supports engaging graphics animation on low-power consumer-electronics devices, delivering performance that is about halfway between a Sony PlayStation-1 and a PlayStation-2. For GPS and other devices in which graphics performance is not of primary importance, the entire screen can be buffered in a unified main memory, thus minimizing gate-count. For devices that require higher graphics performance, local memory for data structures or screen buffering can be included in the graphics engine. Polygon vertices are calculated using the Float16 operand format.

The geometry engine includes three 16-bit multiply-accumulate (MAC) units and a 16-bit floating-point division unit, as shown in Figure 1. The engine can fetch graphics commands from a programmable list, transform vertices, and perform lighting effects autonomously. It supports three directional lights, one ambient light, and three specular lights.

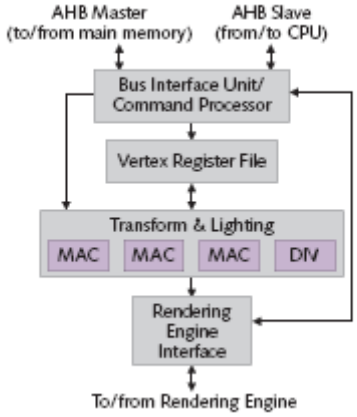

Figure 1.

This implementation of the ZEVIO graphics engine uses only 300,000 gates and consumes only 20mW of power at 75MHz when fabricated in a 0.13-micron process.

3D Sound Processor

The ZEVIO platform also includes an optional 24MHz audio engine with up to 64 audio channels. The audio engine supports a wide variety of stereo sound effects and playback features. Audio output is 16-bit, pulse-code modulation (PCM). Audio input can be 8- or 16-bit PCM or 4-bit adaptive differential PCM (ADPCM).

The audio engine uses large bursts to load data from memory. It processes the data in 32-sample frames, in multiple samples per channel. Volume and pitch controls are independent for each channel, as is gain control of the attack-decay-sustain-release (ADSR) envelope. Drivers are provided for VoIP, MIDI playback, MP3 decode, and compression of sound fonts.

16 of the audio channels can be used for 3D sound to speakers or headphones. The 16 audio channels have special transfer functions that can localize sound at any point in a virtual 3D sound environment. The special functions are supported by 3D history memory within the audio engine. The history memory has 25 16-bit locations for each of the 16 3D audio channels. A cross-talk cancellation filter supports output to the speakers or headphones.

Figure 2 shows a block diagram of the audio engine. The engine requires a digital-to-analog converter either integrated on-chip or connected externally. Echo effects are supported with a programmable reverb filter, allowing implementation of realistic musical-instrument and voice sounds that one would experience in enclosed environments (buildings, cityscapes, caves, etc). The echo effects and the 3D sound effects can be used on MP3-file or digitized-speech inputs. The engine supports the HiFi-2 low-level extensions of the original HiFi engine released in 2003.

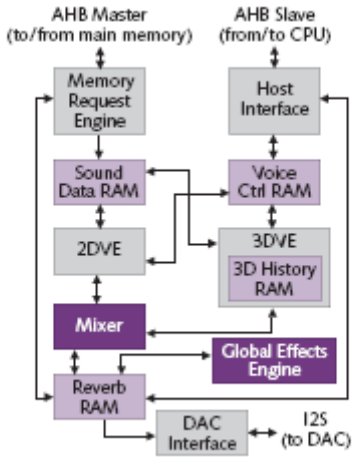

Figure 2.

This implementation of the ZEVIO audio engine uses only 80,000 gates and consumes only 2mW of power at 24MHz when fabricated in a 0.13-micron process. Small audio-processing needs can often be handled by an SoC's host processor, thus avoiding the need for this audio engine.

CONCLUSION

The ZEVIO platform offers a large number of features and options for SoC developers seeking high performance, low power, low cost, and fast time-to-market. The main attraction of the ZEVIO platform is that LSI Logic can become a developer's one-stop shop, whether a turnkey, semi-custom or

fully customized solution is required. The ZEVIO platform makes wise trade-offs to offer the optimal balance for next-generation CE products. For more information about the ZEVIO platform, see http://www.lsi.com/zevio.