NEC

VRC5074 System Controller

Revision 1.0

Data Sheet **June 1998**

1.0 Introduction

1.1 Overview

The VRC5074 System Controller is a software-configurable chip that directly connects the VR5000 CPU to SDRAM memory, a PCI Bus, and a Local Bus, without external logic or buffering. From the CPU's viewpoint, the controller acts as a memory controller, DMA controller, PCI-Bus host bridge, and Local-Bus host bridge. From the viewpoint of PCI agents, the controller acts as master and target on the PCI Bus. The controller also has one serial port and four timers.

1.2 Features

- **CPU Interface**
  - Connects directly to a 250 MHz VR5000 CPU.
  - 100 MHz CPU bus.
  - Peak block-transfer throughput of 800 Mbytes/sec, maximum sustained throughput of 640 Mbytes/sec.
  - 16 x 8-byte (128-byte) CPU-to-controller FIFO.
  - Little-endian or big-endian byte order on CPU interface.
  - Supports secondary cache.
  - 15 interrupt sources, individually enabled and assigned to one of the CPU's seven interrupt inputs.
  - Supports all CPU bus-cycle types (but the only write type is pipelined write). Parity generation and checking on CPU data cycles.
  - Mode data at reset provided by a serial EEPROM or by the controller.
  - 3.3V I/O.
- **Memory Interface**
  - 100 MHz memory bus.
  - Maximum sustained throughput of 800 Mbytes/sec.
  - Supports three physical loads per data bit: two SDRAM physical banks and one other (e.g., EPROM, Flash, or buffers bridging to a secondary memory bus).
  - Supports four types of SDRAM with two to four on-chip virtual banks: 256Mb four-bank, 64Mb four-bank, 64Mb two-bank, 16Mb two-bank.
  - On-chip bank-interleaving buffers.
  - Programmable address ranges for each memory bank.
  - Memory may maintain multiple open SDRAM pages.
  - Parity or ECC generation and checking of memory data cycles with 64+8 bits of SDRAM and no performance degradation.

- Read/write buffers:
  - 8-dword (64-byte) CPU Write FIFO.
  - 8-dword (64-byte) PCI Write FIFO.
- On-chip refresh generation.
- 3.3V I/O.

❑ **PCI Bus**

- Full compliance with *PCI Local Bus Specification, Revision 2.1*.
- Four possible configurations:
  - 66 MHz, 64-bit bus (maximum sustained bandwidth 533 Mbytes/sec)
  - 66 MHz, 32-bit bus (maximum sustained bandwidth 267 Mbytes/sec)
  - 33 MHz, 64-bit bus (maximum sustained bandwidth 267 Mbytes/sec)
  - 33 MHz, 32-bit bus (maximum sustained bandwidth 133 Mbytes/sec)
- PCI-Master support, allowing the CPU, DMA, and Local-Bus masters to access targets on the PCI Bus via two programmable PCI Address Windows.
- PCI-Target support, allowing PCI-Bus masters to access to all controller resources.
  - Eleven programmable Base Address Register (BAR) windows.
  - All reads are delayed transactions.
  - Up to four simultaneous delayed transactions.
- Master and target read/write bursts up to 2 Mbytes in length.
- Master and target read/write buffers:
  - 32-entry x 8-byte (256-byte) PCI Output FIFO.
  - 32-entry x 8-byte (256-byte) PCI Input FIFO.
  - 4-entry x 8-byte (32-byte) CPU Delayed Read Completion (DRC) Buffer.
  - 4-entry x 8-byte (32-byte) DMA Delayed Read Completion (DRC) Buffer.
- Optional PCI Central Resource functions:
  - Buffered PCI clock to 5 other PCI devices.
  - PCI clock can be external or derived from CPU clock.
  - Arbitration for the controller and 5 other PCI devices.
  - CPU interrupt control for 5 PCI devices.
- Full PCI Configuration Space.
- 64-bit addressing support for master and target using Dual Address Cycle (DAC).
- Locked cycle (exclusive access) support as master and target.
- Parity generation and checking on address and data cycles.
- Compliant with both 3.3V and 5V PCI signaling.

❑ **Local Bus**

- 25 MHz or 50 MHz bus (0.25 or 0.50 of system clock).
- Programmable chip-selects for 7 devices plus Boot ROM.
  - Each chip-select supports up to 4GB address space.
  - Devices may alternatively be located on the memory bus.
  - Chip-select signals may alternatively be used for DMA or UART control, or as general-purpose I/O signals.
- Support for burst cycles on the Local Bus.

- Support for Local-Bus master control of the Local Bus, using 68000 or Intel arbitration protocols.
- Programmable control-signal relationships and timing:
  - Timing can be fixed or use external Ready signal.
  - 12-bit timer for external Ready signal.
- 3.3V outputs, 5V-tolerant inputs

❑ **DMA**

- Two DMA channels.
- Block transfers to or from any physical address.
- Transfers initiated by the CPU, a PCI-Bus master, or a Local-Bus master.
- Peak block-transfer throughput of 800 Mbytes/sec, maximum sustained throughput of 640 Mbytes/sec.
- 32 x 8-byte (256-byte) DMA FIFO.
- Two sets of DMA control registers. One set can be programmed while the other performs a transfer.
- Chained transfers—when one transfer completes, another programmed transfer automatically begins.
- Supports bidirectional, unaligned transfers.
- Optional hardware handshake signals (REQ#, ACK#, EOT#) if certain chip-selects are not used.

❑ **Serial Port (UART)**

- Compatible with National Semiconductor's PC16550D UART.
- Receiver and transmitter each have a 16-byte FIFO.
- 5, 6, 7, or 8 bits per character.
- Even, odd, or no parity-bit generation and detection.
- 1, 1.5, or 2 stop-bit generation.
- Baud-rate generator division of input clock by 1 to (2^{16} -1).
- Prioritized interrupt controls.
- DSR and DTR control signals.
- Optional hardware controls (CTS#, RTS#, DCD#, XIN#) if certain chip-selects are not used.

❑ **Timers**

- 16-bit SDRAM refresh timer.
- 24-bit CPU-bus read timer.
- 32-bit general-purpose timer.
- 32-bit watchdog timer.
- All timers are cascadable.

❑ **Multi-Controller Support**